Hall Ticket No.:

NARSIMHA REDDY ENGINEERING COLLEGE
(UGC AUTONOMOUS)

MODEL QUESTION PAPER

II B.Tech II Semester (NR21) Regular Examination, February 2023
Digital Electronics
(Electrical and Electronics Engineering)

Time :3 hours   **Maximum marks: 70**

Note:
- This question paper contains two parts A and B
- Part A is compulsory which carries 20 marks (10 sub questions are two from each unit carry 2 Marks). Answer all questions in Part A
- Part B Consists of 5 Units. Answer any one full question from each unit. Each question carries 10 Marks and may have a, b sub questions

Part-A   (20 Marks)
Answer all questions

Q.No		Question	M	CO	BL	PO
1)	a.	**Write** short notes on binary number systems.	2	1	1	1
	b.	**Differentiate** between binary code and BCD code.	2	1	3	2
	c.	**Sketch** the following logic function using k-map and implement it using logicgates? Y(A,B,C,D)= Σm(0,1,2,3,4,7,8,9,10,11,12,14)	2	2	3	3
	d.	**Explain** how combinatorial circuits differ from sequential circuits.	2	2	2	1
	e.	**Define** a Flip-Flop?	2	3	1	1
	f.	**Illustrate** applications of shift registers.	2	3	3	3
	g.	Write short notes on R-2R Ladder D/A converter	2	4	1	1
	h.	Define specifications of A/D converters	2	4	1	1
	i.	Draw the static and dynamic RAM cells.	2	5	6	1
	j.	What is PLA? How does it differ from PAL and GAL?	2	5	4	2

Part-B   (50 Marks)
Answer any five questions
All Questions carry equal Marks

Q.No		Question	M	CO	BL	PO
		UNIT−I				
2)	a.	Construct a table for 4 -3 -2 -1 weighted code and write 9154 using this code .	5	1	4	3
	b.	Explain what do you mean by error detecting and correcting codes?	5	1	2	1
		OR				

3)	a.	Compare & contrast the features of TTL & CMOS logic families.	5	1	4	2
	b.	Draw the schematic and explain the operation of a CMOS inverter. Also explain its characteristics.	5	1	1	3

UNIT–II

4)	a.	**Design** a 4-bit binary to BCD converter.	5	2	1	3
	b.	**Design** a full adder using two half adders.	5	2	1	3

OR

5)	a.	Simplify the following Boolean functions, using a four variable Karnaugh map method and implement the simplified function using NAND gates. F(A,B,C,D) = Σ0,2,4,5,6,7,8,10,13,15)	5	2	3	2
	b.	**Design** the block diagram of a 4:1 multiplexer using 2:1 multiplexer.	5	2	1	2

UNIT–III

6)	a.	**Write** short notes on shift register? Mention its application along with the Serial Transfer in 4-bit shift Registers.	5	3	2	1
	b.	Design 4-bit shift register using D flip-flops	5	3	2	3

OR

7)	a.	**Design** a MOD-5 synchronous counter using flip flops and implement it? Also draw the timing diagram. .	5	3	2	2
	b.	**Design** Johnson counter and state its advantages and disadvantages.	5	3	2	2

UNIT–IV

8)	a.	Explain the working of R-2R ladder DAC with neat circuit diagram and mention it's limitations.	5	4	2	1
	b.	What is the major disadvantage of the digital ramp type ADC?	5	4	1	1
9)	a.	Design a 3-bit paraller-comparator A/D converter for 2's complement format.	5	4	2	2
	b.	Describe the operation of a DAC.	5	4	4	1

UNIT–V

10)	a.	Give the classification of semiconductor memories	5	5	1	1
	b.	Write short note on RAM, types of ROMs	5	5	1	2
11)	a.	Implement the following function using PLA F1=Σ (0, 1, 2, 4) and F2 = Σ (0, 5, 6, 7).	5	5	2	3
	b.	Implement the following Boolean function using 3×4×2 PLA, F1(x, y, z) = Σ (0, 1, 3, 5) and F2(x, y, z) = Σ (3, 5, 7)	5	5	2	3

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M – Marks   **CO –** Course Outcomes   **PO –** Program Outcomes

BL – Bloom's Taxonomy Levels (**L1–**Remembering, **L2–**Understanding, **L3–**Applying, **L4–**Analyzing, **L5–**Evaluating, **L6–**Creating)